AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-33. (Canceled without prejudice or disclaimer).

34. (Original) A process for producing a nonvolatile semiconductor memory device comprising a plurality of memory cells each having a floating gate formed on a semiconductor substrate with the interposition of a tunnel dielectric film and a control gate formed on said floating gate with the interposition of an interpoly dielectric film, and a plurality of field effect transistors each having gate electrodes formed on the semiconductor substrate with the interposition of a gate insulating film, said process comprising the steps of:

forming a shallow groove isolation region on a semiconductor substrate;

forming a tunnel dielectric film on the semiconductor substrate surface in said memory cell formed region by thermal oxidation method,

depositing a first polycrystalline Si film which becomes said floating gate, and then removing the first polycrystalline Si film in said field effect transistor formed region;

depositing a first silicon oxide film which becomes the first portion of said gate insulating film, and then removing the first silicon oxide film in said memory cell formed region;

depositing a second silicon oxide film which becomes said interpoly dielectric film and a second portion of said gate insulating film; and

depositing a second polycrystalline Si film which becomes said control gate and said gate electrodes.

35. (Original) The process according to claim 34 wherein in the fourth and fifth steps, the first and second silicon oxide films just after deposition are annealed in an NH3 atmosphere and further subjected to wet oxidation.

36. (Original) The process according to claim 34 wherein in the third and sixth steps, the first and second polycrystalline Si films are doped with phosphorus.

37. (Original) A process for producing a nonvolatile semiconductor memory device comprising a plurality of memory cells each having a floating gate formed on a semiconductor substrate with the interposition of a tunnel dielectric film and a control gate formed on said floating gate with the interposition of an interpoly dielectric film, and a plurality of field effect transistors each having gate electrodes formed on the semiconductor substrate with the interposition of a gate insulating film, said process comprising the steps of:

forming a shallow groove isolation region on the semiconductor substrate;

forming a tunnel dielectric film on the semiconductor substrate surface in the memory cell formed region by thermal oxidation method;

depositing a first polycrystalline Si film which becomes said floating gate, and then removing the first polycrystalline Si film in said field effect transistor formed region;

forming a first silicon oxide film, which becomes a first portion of said gate insulating film, on the semiconductor substrate surface in the field effect transistor formed region by thermal oxidation method;

depositing a second silicon oxide film which becomes said interpoly dielectric film and a second portion of said gate insulating film; and

depositing a second polycrystalline Si film which becomes said control gate and said gate electrodes.

38. (Original) The process according to claim 37 wherein in the fifth step, the second silicon oxide film just after its deposition is annealed in an NH_3 atmosphere and further subjected to wet oxidation.

39. (Original) The process according to claim 37 wherein in the third and sixth steps, the first and second polycrystalline Si films are doped with phosphorus.

40. (Original) A process for producing a nonvolatile semiconductor memory device comprising a plurality of memory cells each having a floating gate formed on a semiconductor substrate with the interposition of a tunnel dielectric film and a control gate formed on said floating gate with the interposition of an interpoly dielectric film, and a plurality of field effect transistors each having gate electrodes

formed on the semiconductor substrate with the interposition of a gate insulating film, said process comprising the steps of:

forming a shallow groove isolation region on a semiconductor substrate;

depositing a first silicon oxide film which becomes a first portion of said gate insulating film, and then removing said first silicon oxide film in the memory cell formed region;

forming a tunnel dielectric film on the semiconductor substrate surface in the memory cell formed region and forming a second silicon oxide film which becomes a second portion of said gate insulating film between said semiconductor substrate in the transistor formed region and said first silicon oxide film, both by thermal oxidation method;

depositing a first polycrystalline Si film which becomes said floating gate and said gate electrodes;

depositing a third silicon oxide film which becomes said interpoly dielectric film; and

depositing a second polycrystalline Si film which becomes said control gate.

41. (Original) The process according to claim 40 wherein in the second and fifth steps, the first and third silicon oxide films immediately after their deposition are annealed in an NH_3 atmosphere and further subjected to wet oxidation.

42. (Original) The process according to claim 40 wherein in the fourth and sixth steps, the first and second polycrystalline Si films are doped with phosphorus.

43. (New) A process according to claim 37, wherein said second silicon oxide film is formed over said first silicon oxide film so that said gate insulating film comprises a laminated film of said second portion formed over said first portion.

44. (New) A process according to claim 39, wherein said second silicon oxide film is formed over said first silicon oxide film so that said gate insulating film comprises a laminated film of said second portion formed over said first portion.